



# Evaluating performance limiting defects in novel thin-film materials for solar cells

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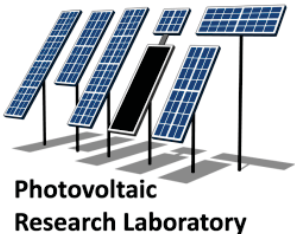
# Evaluating performance limiting defects in novel thin-film materials for solar cells

Fall MRS – December 201

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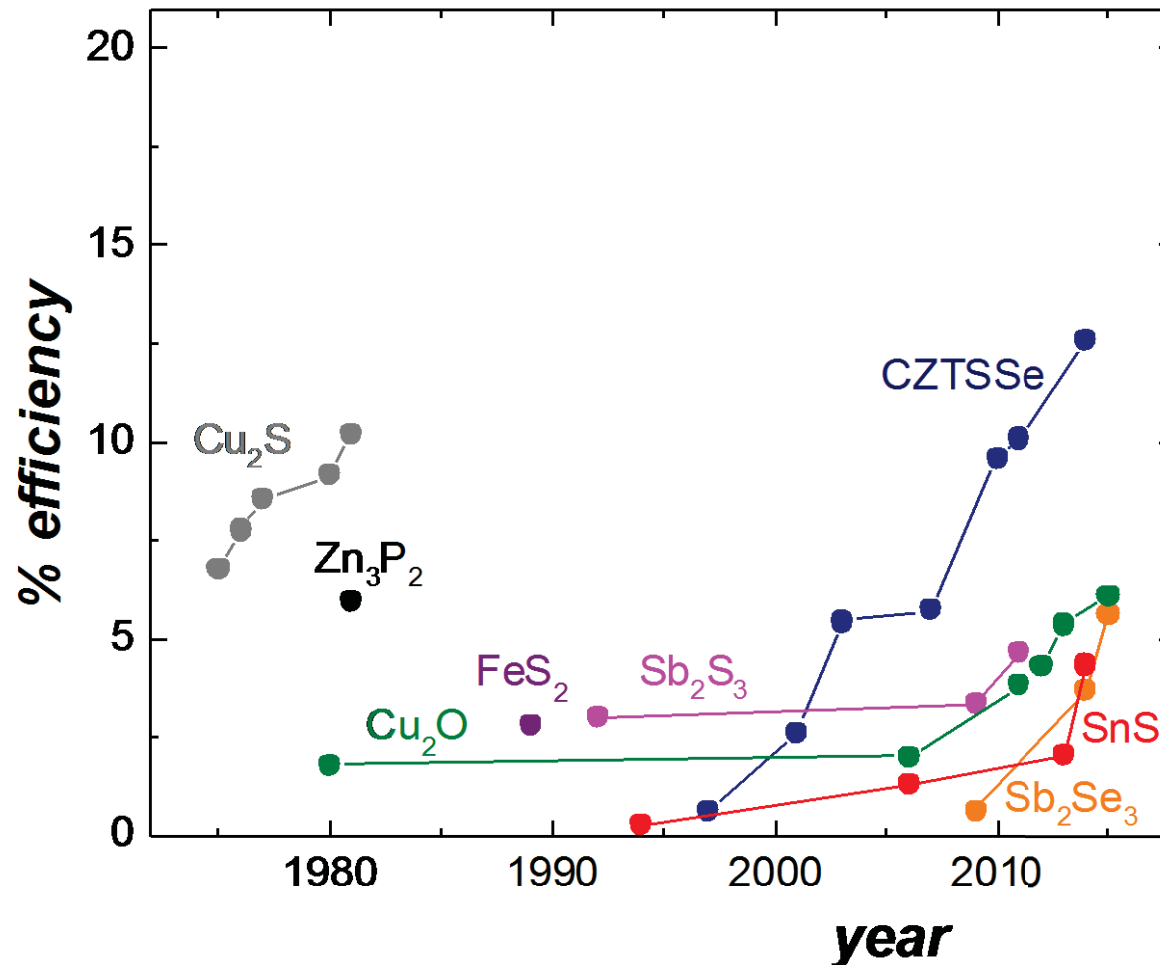
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# Development of novel Earth-abundant solar cells

- Many inorganic thin-film materials are underperforming (< 10% laboratory efficiency) despite decades of R&D.

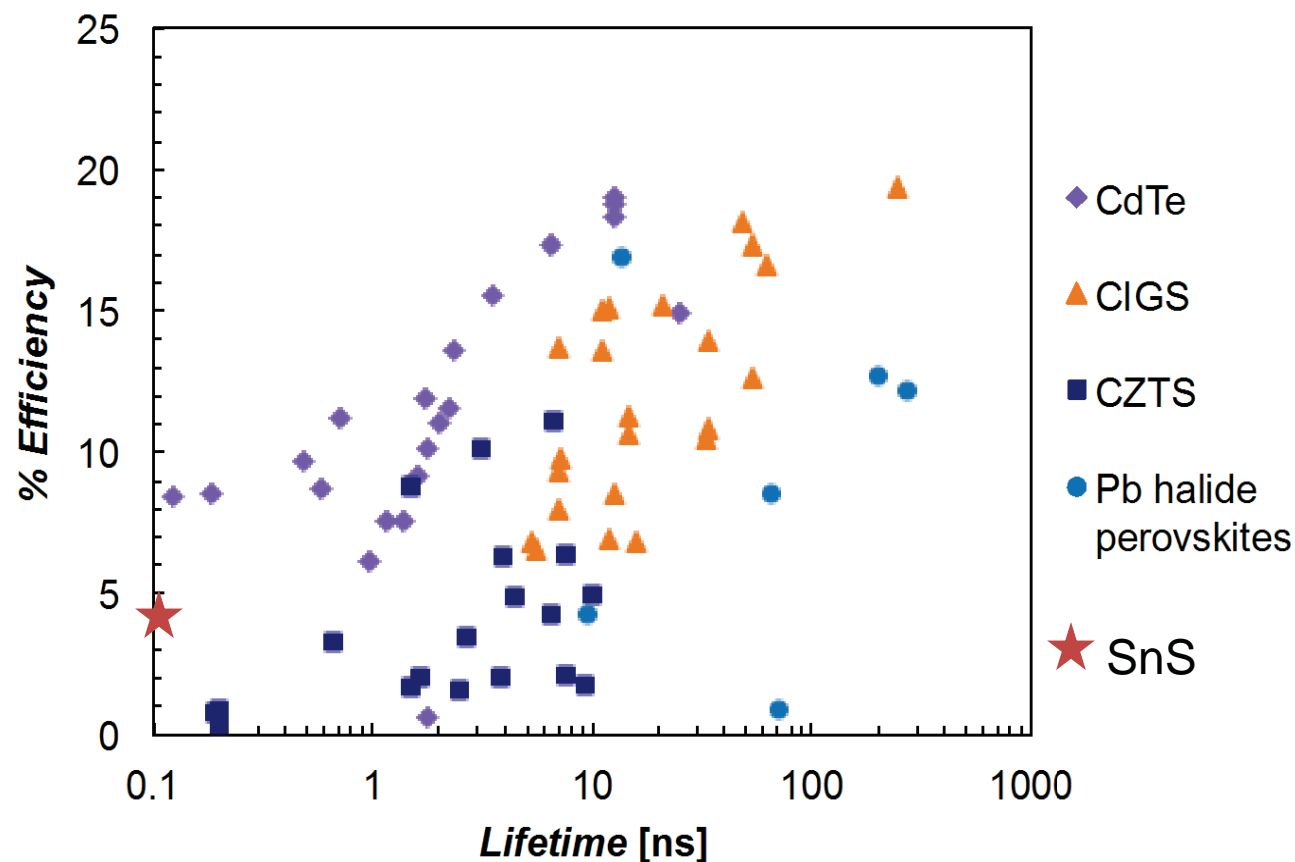


V. Steinmann *et al.*, *Nature Photonics* **9**, 355 (2015).

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# High bulk carrier lifetime for high-performance devices

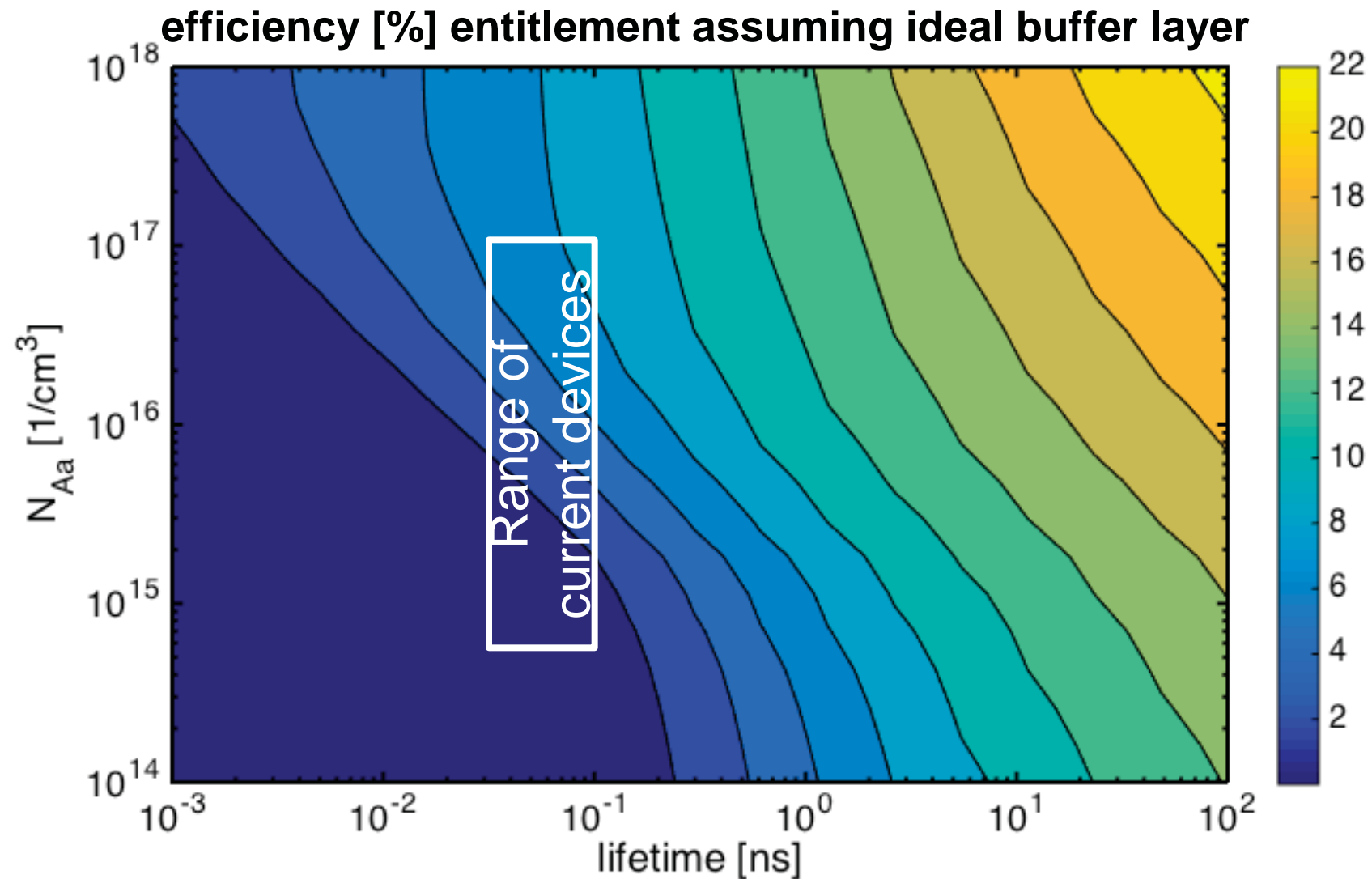
- High bulk carrier lifetime ( $> 1\text{--}10\text{ ns}$ ): a pre-requisite for high conversion efficiencies ( $\geq 10\%$ ).



R. Jaramillo *et al.*, submitted (2015).

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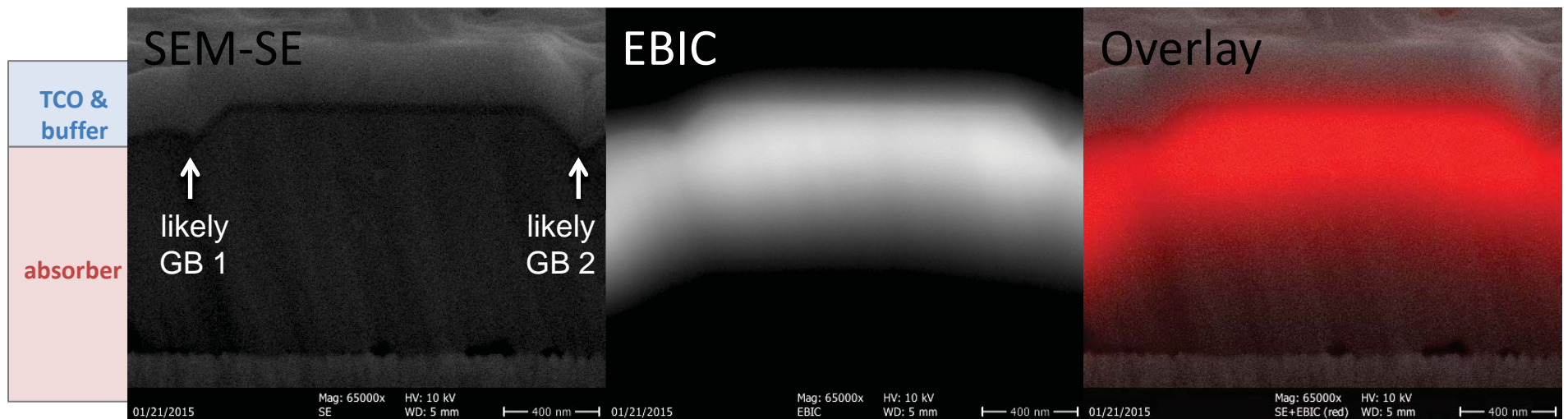
# Bulk carrier lifetime in SnS



# What defects limit the SnS device performance?

- We perform cross-sectional SEM and electron-beam-induced current (EBIC) to study the thin-film morphology and electronic activity.
- Intragranular recombination appears to limit bulk carrier lifetime/diffusion lengths, caused by:
  - Extrinsic defects (impurities)
  - Extended structural defects (stacking folds, dislocations).

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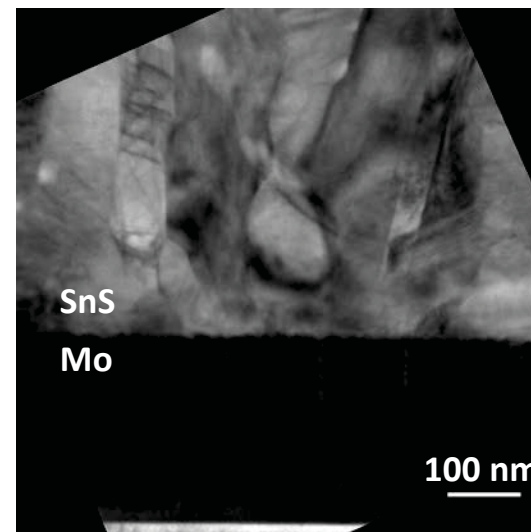


V. Steinmann *et. al.*, under preparation.

# Extended structural defects in SnS

- Transmission electron microscopy (TEM) reveals high density of intragranular extended structural defects at  $T_{\text{substrate}} \sim 0.5 T_{\text{melt}} (< 450^\circ \text{ C})$ .
- Hypothesis: higher temperature growth may help to reduce the extended structural defect density and improve charge carrier diffusion length.

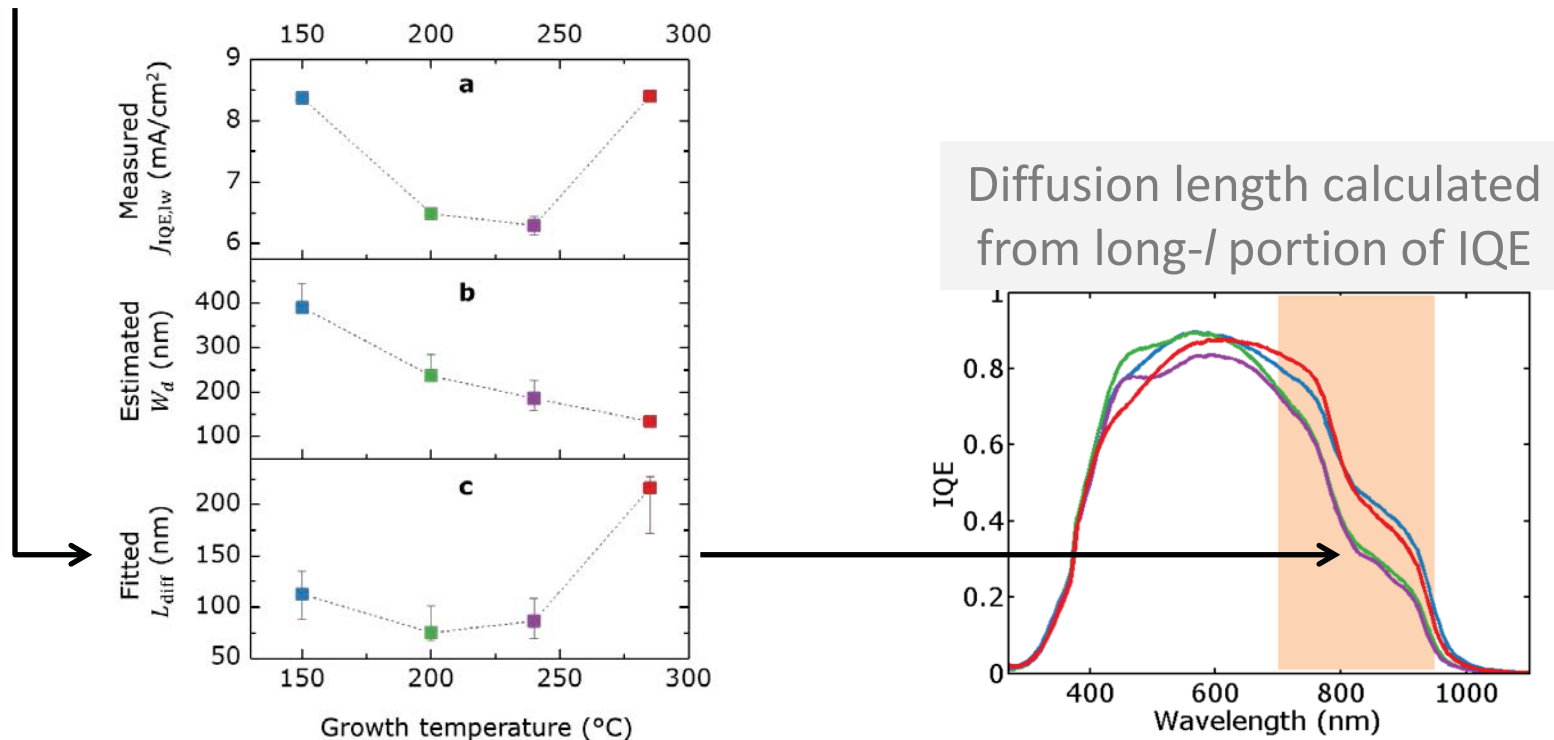
Growth temperature  $< 300^\circ \text{ C}$ ,  
annealing temperature  $< 450^\circ \text{ C}$



SnS melting point at  $T_{\text{melt}} = 882^\circ \text{ C}$ .

# First results show increase in diffusion length

- Explored range of growth temperatures from 150–285° C, annealed at 400° C in 4% H<sub>2</sub>S ambient.
- Diffusion length increases with higher growth temperature.



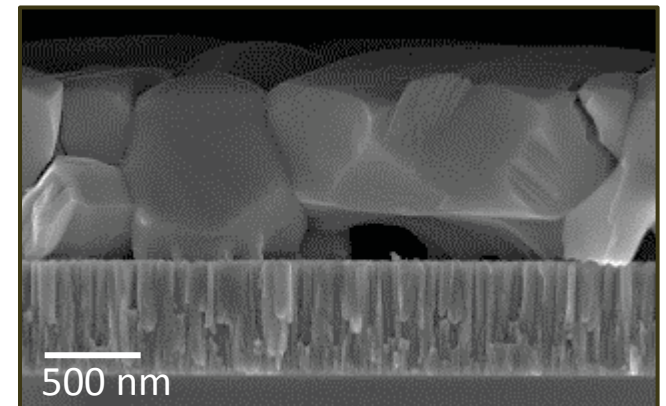
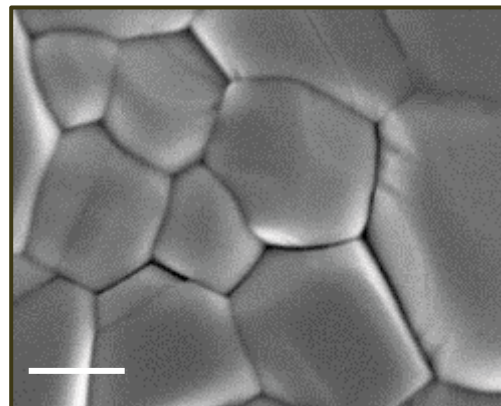
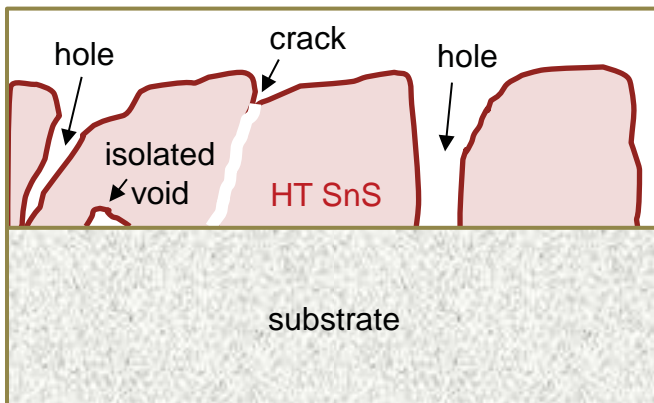
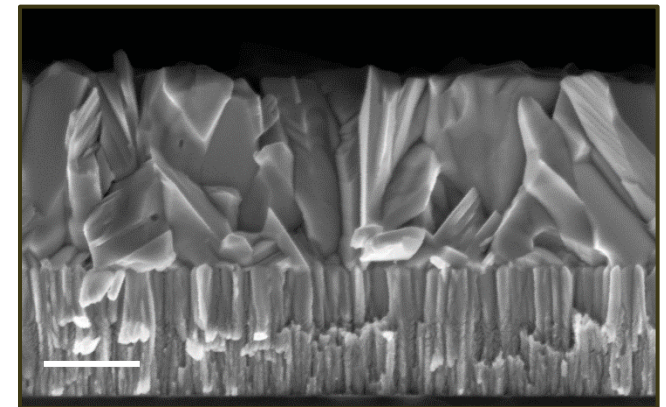
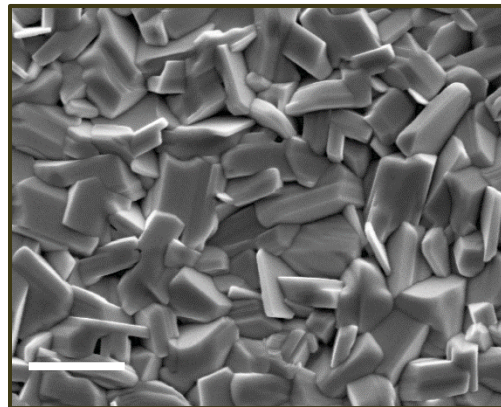
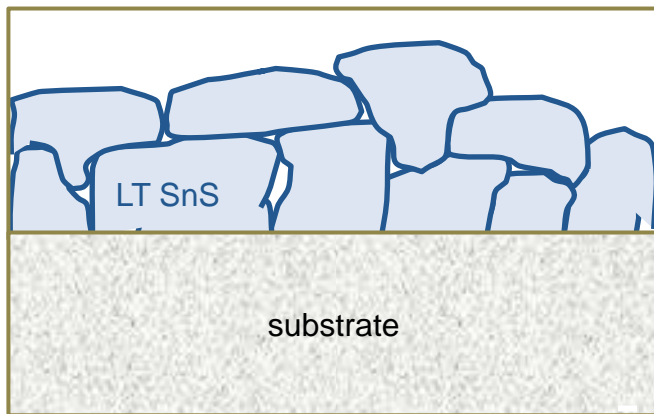
R. Chakraborty, V. Steinmann *et al.*, *Appl. Phys. Lett.* 2015.

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# High-temperature processing causes cracks

- locally unfavorable surface energetics and/or coefficients of thermal expansion make polycrystalline SnS with many different grain orientations especially prone to through-thickness voids.

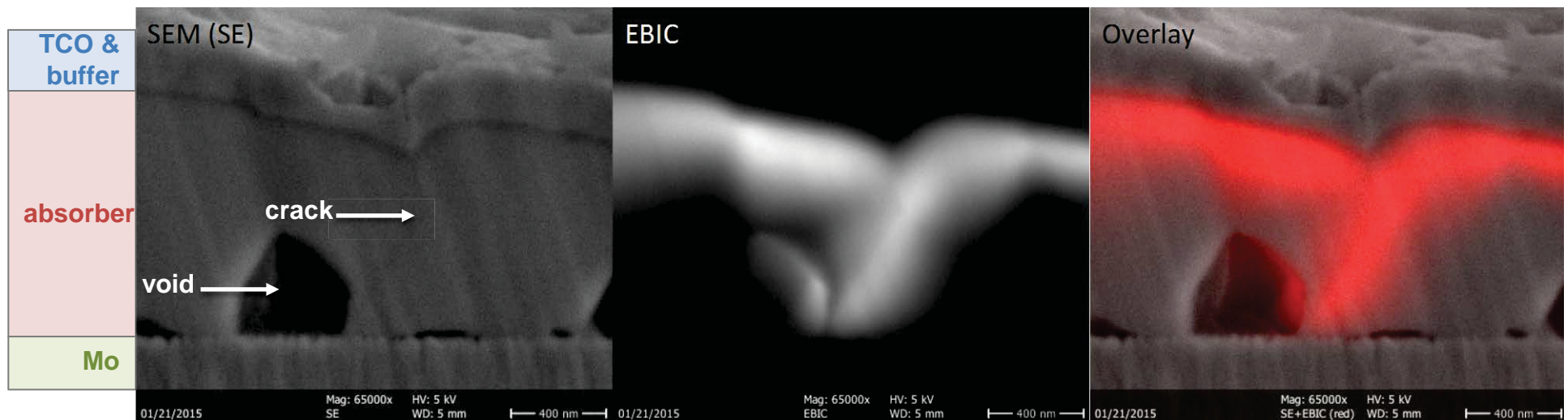


V. Steinmann *et. al.*, under preparation.

LT: low-temperature, HT: high-temperature MRS 2015 – Vera Steinmann

# High-temperature processing causes cracks

- Cross-sectional electron-beam-induced current (EBIC):
- Cracks can become current pathways vertically across SnS absorber layer → leading to shunts in devices.

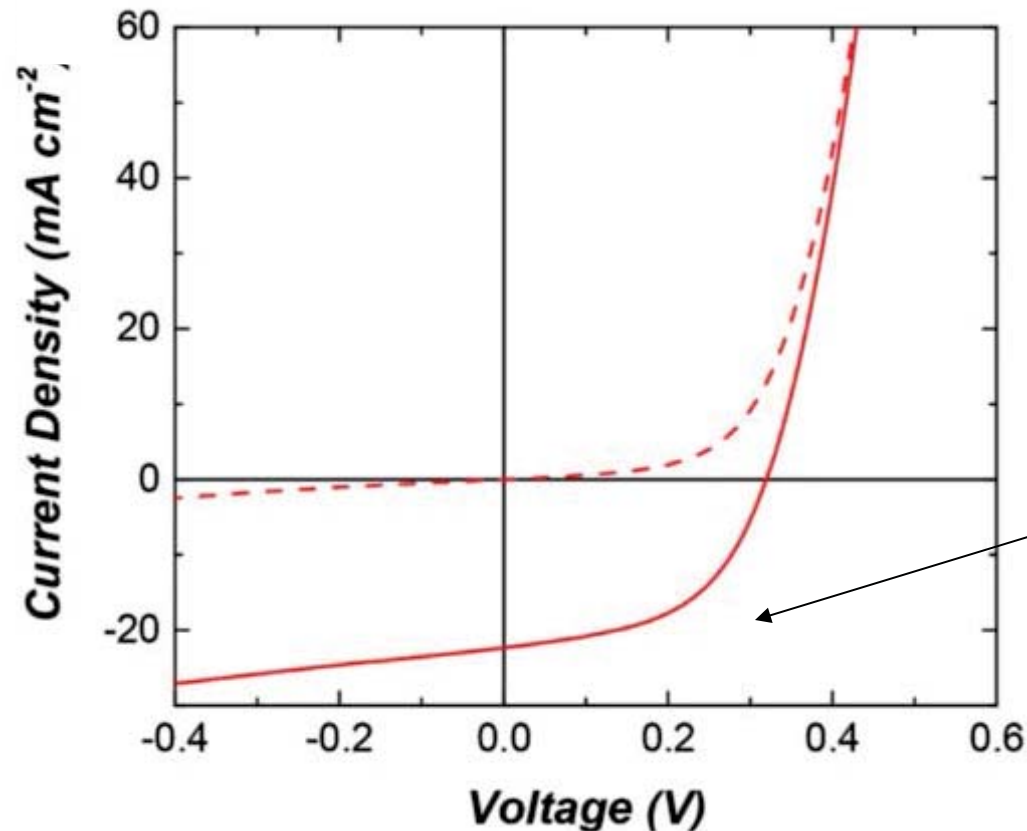


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# Shunting in SnS solar cells

- Cracks across the SnS bulk contribute to low shunt resistance in devices.



$$R_{\text{shunt}} = 74 \, \Omega \, \text{cm}^2$$
$$R_{\text{series}} = 0.66 \, \Omega \, \text{cm}^2$$

Evidence of shunting in  $J$ — $V$  characteristics.

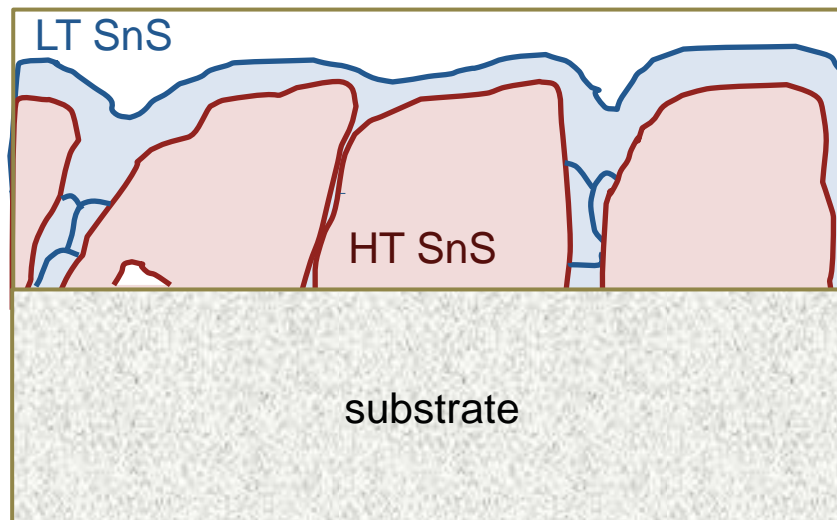
$$V_{OC} = 334.1 \, \text{mV}, J_{SC} = 20.6 \, \text{mA/cm}^2, FF = 65.28\%, PCE = 3.88\%$$

V. Steinmann *et al.* *Adv. Mater.* 26, 7488 (2014).

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# Two step deposition approach to avoid shunts

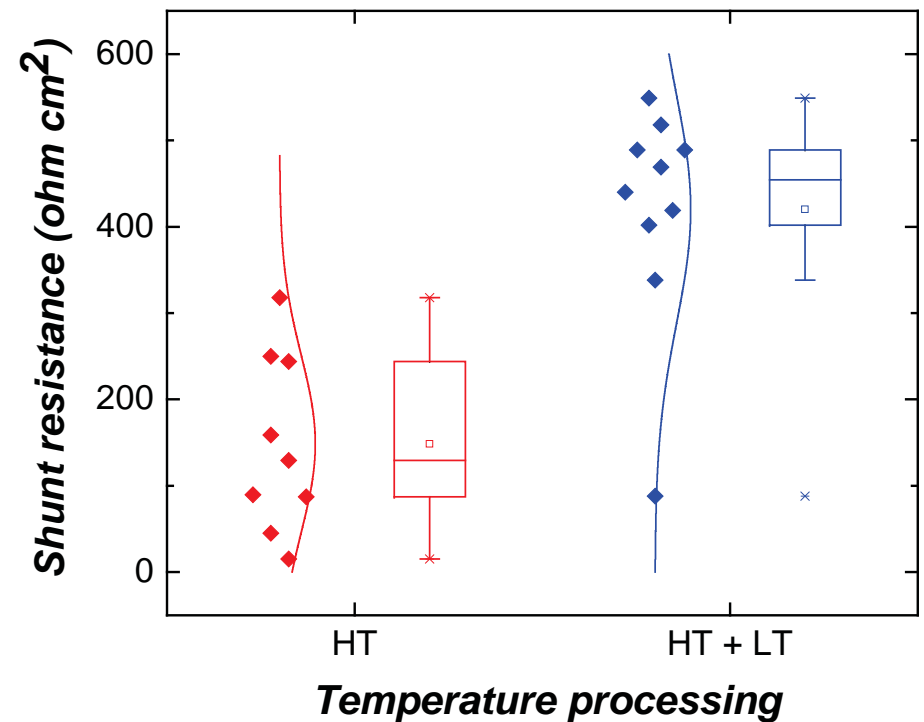
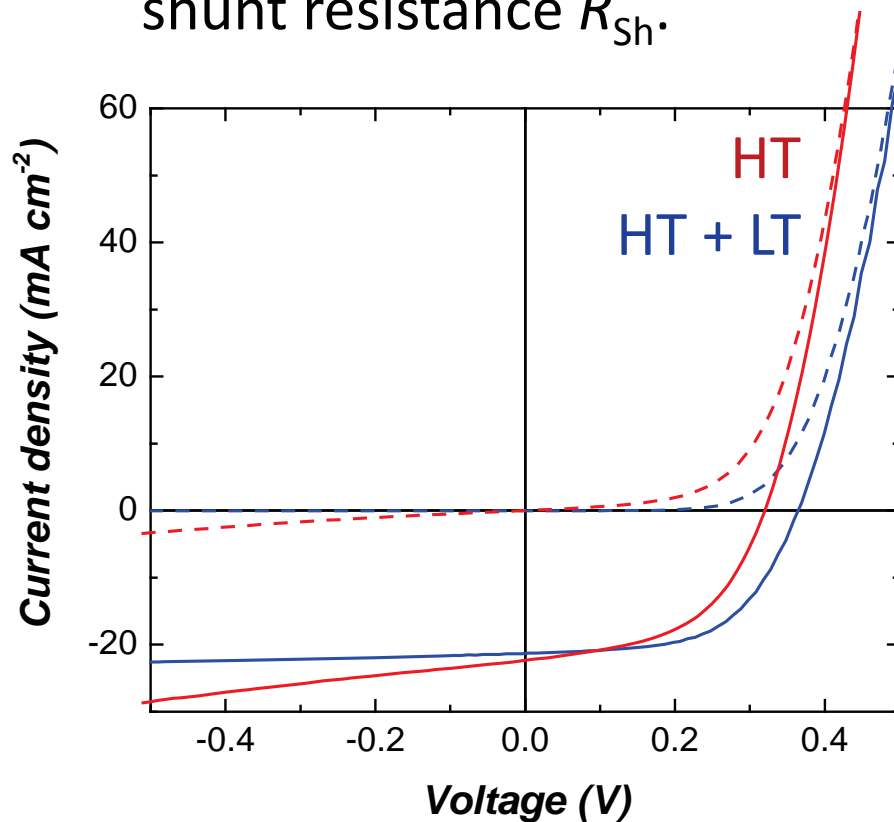
- Apply continuous thin absorber coverage at low-temp. to reduce number of shunted devices.
- High-temp. anneal at 400° C + low-temp. deposition at 240° C.



LT: low-temperature  
HT: high-temperature

# Shunt reduction by two step deposition approach

- Improved fill factor and open-circuit voltage due to improved shunt resistance  $R_{Sh}$ .



V. Steinmann *et. al.*, under preparation.

# Take-aways

- High bulk carrier lifetime is necessary (but not sufficient) for high-efficiency solar cells.
- Lifetime in SnS thin-films is limited by intragranular recombination.
  - Extrinsic defects
  - Extended structural defects
- High-temperature processing can reduce extended structural defect density and improve SnS bulk carrier lifetime.
- High-temperature processing causes cracks in SnS thin-film, leading to shunts in devices.
- Two step absorber deposition approach successfully “plugs holes” and improves shunt resistance in devices.

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